ELSEVIER

Sensors and Actuators A 67 (1998) 109–114

SENSORS AND ACTUATORS A PHYSICAL

Progress in VLSI optical position-sensitive circuits

Marco Tartagni [a,*], Pietro Perona [b,c]

[a] DEIS, University of Bologna, viale Risorgimento 2, I-40136 Bologna, Italy
[b] California Institute of Technology 136-93, Pasadena, CA 91125, USA
[c] DEI, University of Padua, via Gradenigo 6/a, I-35131 Padua, Italy

Abstract

This paper describes new techniques to implement 1-D and 2-D mesh-type position-sensitive devices (PSDs) using current-mode analog VLSI (very large scale integration). By taking advantage of local analog computation, this approach allows sensors to be merged on the same chip with extremely compact circuits that process the incoming signal. The presented schemes have advantages over conventional implementations in using general-purpose technology and in their capability to be electronically tunable. Three versions of the sensor have been implemented and tested, showing non-linearity r.m.s. errors ranging from 0.1 to 1.2% depending on the architecture.

Keywords: Smart sensors; Optical sensors; Position-sensitive detectors; VLSI

1. Introduction

The application of optical sensors to determine the position and the alignment of objects has increased. Position-sensitive devices (PSDs) are optoelectronic sensors that provide continuous position data of light spots traveling over their photosensitive surfaces. The main advantages of PSDs over digital implementations are simultaneity of 2-D measurements and simplicity in circuitry, which allow useful applications for autofocus systems, displacement and vibration monitors, optical position and remote control systems. Mesh-type PSDs (MEPSDs) have shown advantages over uniform resistive layers in the linearity and time response of the position detection, but the price paid is the use of customized fabrication processes, such as p-i-n structured devices, and the requirement for off-chip data computation [1]. Integrated microcircuits have been proposed to find the centroid [2] by means of analog computation, though they still require a customized process for accurate setting of sheet resistance values and the use of JFET devices. Other embedded systems [3] have been proposed, which make use of sophisticated sigma–delta data converters.

Over the past few years, the construction and demonstration of analog very large scale integration (VLSI) visual processing systems have made enormous progress. In pursuing the idea of implementing neuromorphic systems [4], the constraint of the medium has driven the developments of new concepts and devices. Thus, several successful implementations of micropower collective-computational systems have been demonstrated [5]. A collective-computational system for detecting the center of mass and higher-order moments [6] of images of bright objects has been reported. However, the proposed circuit is complex and area expensive. Recently, an integrated device [7] has been proposed as a dedicated optical front-end for solar illumination monitoring. However, the device is tailored to a specific application and does not perform contrast normalization as proposed by our approach.

In this paper we show that current-mode analog techniques implemented in general-purpose BiCMOS (bipolar complementary metal oxide silicon) technology can perform sophisticated on-chip computation with a high degree of precision. In Section 2 we propose a simple and compact position-sensing circuit and we discuss an edge-sensitive version based on the same architecture. In Section 3 we discuss implementations and measurements.

2. Theory

The well-known idea underlying the position-sensitive device is described in Fig. 1(a). For a discrete 1-D uniform resistive grid the coordinate of injection of a current (i.e., coming from a photodiode) is

* Corresponding author. Tel.: +39-51-644-3557; Fax: +39-51-644-3073; E-mail: mtartagni@deis.unibo.it

0924-4247/98/$19.00
PII S0924-4247(97)01773-1

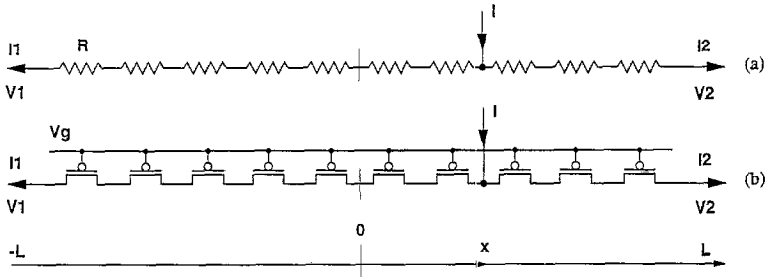

Fig. 1. Resistive and pseudo-resistive networks.

$$\frac{x}{L}=\frac{n-m}{n+m}=\frac{I_2-I_1}{I_2+I_1}+2\frac{V_2-V_1}{I(n+m)R} \quad (1)$$

where n and m are the number of elements on the left and right side of the point x where the current is injected, L is the length of the sensor and R is the device resistance value. The function $(I_2-I_1)/(I_2+I_1)$ represents a good estimate of x/L as long as the voltage-dependent term of Eq. (1) may be neglected. This requirement may be met for low values of injected current provided that R is large. Extrapolating the concept for a distribution of injected currents $I(k)$ and assuming $V_1=V_2$, it can also be shown that the $(I_2-I_1)/(I_2+I_1)$ function encodes the normalized first moment of $I(k)$, also called the 'centroid' of the current distribution along the chain [6]. This concept can be easily extended in the 2-D space to get the coordinates of the first moment of the current distribution. In this case, the currents conveyed from the corners of a grid-like resistive network contain the information regarding the centroid position. Application of this concept will be shown in the next section.

In a previous work [8] we proposed the approach described in Fig. 1(b) where the resistor chain has been substituted by a chain of MOS transistors. This scheme has the advantages of simplicity over other circuits and of small area by using passive polysilicon resistive layers to implement R. This leads to the following expression for the node location x:

$$\frac{x}{L}=\frac{n-m}{n+m}=\frac{I_2-I_1}{I_2+I_1}+2\frac{K(f(V_g,V_2)-f(V_g,V_1))}{I(n+m)} \quad (2)$$

where K is the aspect ratio and the expression for $f(V_g,V_i)$ depends on the bias region of the MOS transistor [9]. Referring to Eq. (2), note that if $V_1=V_2$ the voltage-dependent term can be canceled out so that the final expression is again $(I_2-I_1)/(I_2+I_1)$ and it is valid in all operating regions of the MOS transistors: strong inversion, weak inversion, linear region, and saturation. Moreover, V_g plays the important role of setting the time constant of the system [8].

To compute the $(I_2-I_1)/(I_2+I_1)$ function, a BiCMOS circuit has been designed as follows. Two current-controlled current conveyor circuits (M3, M4, M5, and M6 of Fig. 2) keep the same boundary voltages, allowing currents to flow down into B3 and B4 collectors without mismatches due to current mirrors. The $(I_2-I_1)/(I_2+I_1)$ ratio is computed by the configuration of B1, B2, B3, and B4 illustrated in Fig. 2 where each transistor can be thought of as a translinear element, that is, a device with a linear relationship between transconductance and current [10]. More specifically, the translinear principle can be stated as follows:

In a closed loop containing an equal number of oppositely connected translinear elements, the product of the current densities in the elements connected in one direction is equal to the corresponding product for elements connected in the opposite direction.

Using the above principle on the loop made of the four mentioned transistors, one may see that the output current, I_o, is equal to $I_{C5}(I_2-I_1)/(I_2+I_1)$, thus giving the required function normalized to the collector current of B5. Note that the above circuit topology, due to the low photodiode current level, can also be implemented by using MOS transistors working in the subthreshold region. In fact, MOS transistors show an exponential function of the drain current versus the gate voltage, thus behaving as a translinear element. However, as soon as the input current approaches the above-threshold region, the translinear principle does not apply and the desired function cannot be achieved. For this limiting reason, this approach has been abandoned.

Conventional PSDs might be used in tracking the position of a bright spot in a dark background since they can identify the center of mass of the bright shape. Nevertheless, very interesting image patterns such as a moving dark bar or a black spot in a white background (i.e., eye pupils or iris) cannot be well tracked since the PSD only follows the first-order moment of the brightness function. This problem is illustrated in Fig. 3 for 1-D and 2-D functions. In Fig. 3(a) is shown a bright spot along with its center of mass, centered on the circular shape. Conversely, the first-order moment of

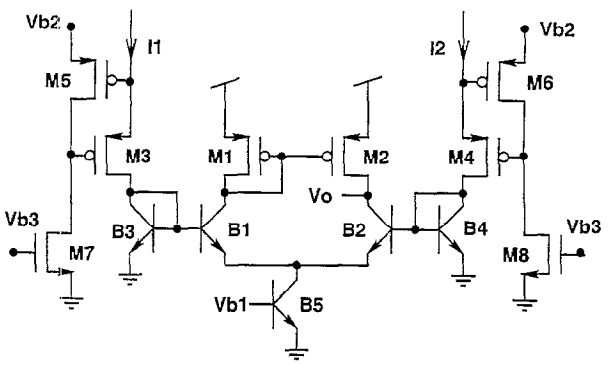

Fig. 2. The $(I_2-I_1)/(I_2-I_1)$ function circuit.

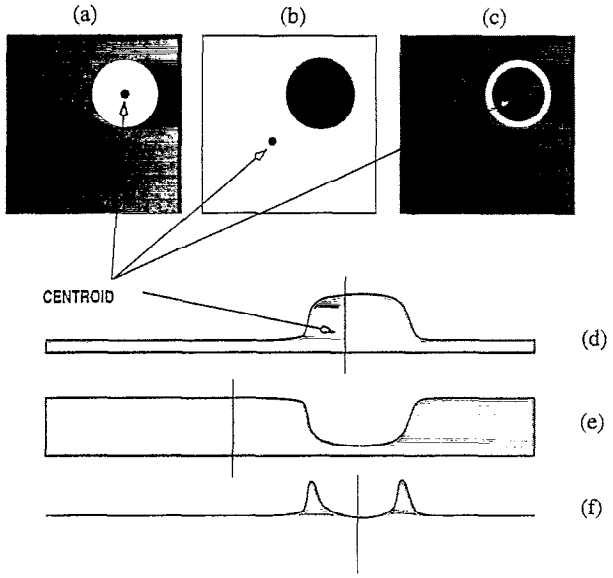

Fig. 3. Edge-sensitive approach.

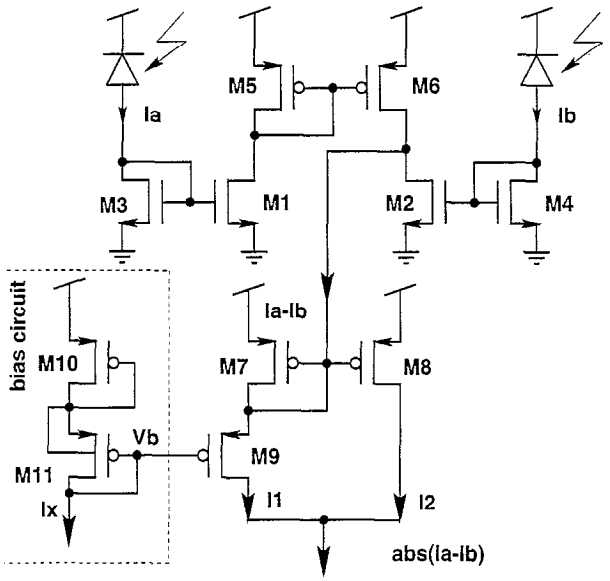

Fig. 4. Absolute-value circuit.

the 'negative' image falls slightly away from the image center, as shown in Fig. 3(b). This behavior impairs the tracking ability of PSDs, thus reducing their applications. To overcome this problem we propose to use analog VLSI for carrying out simple preprocessing in mesh-type PSDs. Fig. 3(c) shows the previous images preprocessed by using the absolute value of the gradient of the image function. The result is the same for both images (a) and (b) and the centroid is correctly placed on the center of the object. A cross section of the previous images is shown in Fig. 3(d–f), illustrating the concept in the 1-D case. More specifically, Fig. 3(d) illustrates another advantage of the contrast normalization previously introduced. In fact, if the background level is not negligible, the centroid tends to move from the circular shape center to the center of the image. Thus, the effect of the flat background can be minimized by using the differential information between adjacent pixels.

A simple circuit that can perform the above-mentioned contrast normalization is illustrated in Fig. 4. Two photodiode currents coming from adjacent photodiodes are mirrored and the resulting current is sinked into an absolute-value circuit [11] composed of M7, M8, and M9. If the $I_a - I_b$ current is positive, M7 turns off so that it can flow down into M9. Conversely, if $I_a - I_b$ is negative, M9 turns off so that M7 and M8 mirror it down into the common node. The current relationship of the circuit can also be explained as follows. Therefore, concentrating on transistors M7, M9, M10, and M11, we identify a translinear loop so that:

$$I_x I_x = I_1 (I_1 - I_{BD})$$

where $I_{BD} = I_a - I_b$. A second equation can be obtained by observing that transistors M7 and M8 form a simple current mirror:

$$I_2 = I_1 - I_{BD}$$

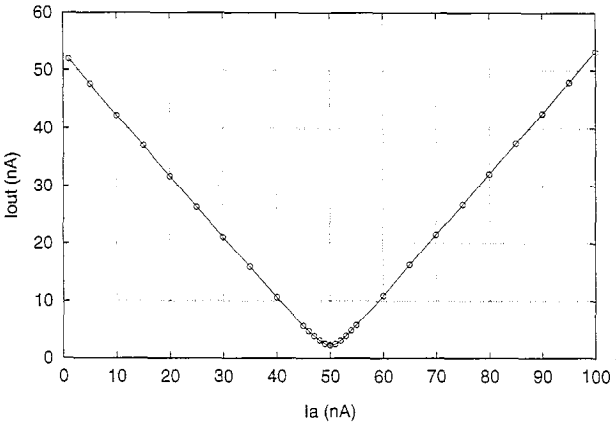

Fig. 5. Absolute-value circuit simulations. $I_b = 50$ nA, $I_x = 70$ nA, all aspect ratios $W/L = 6/4$.

These equations may be solved for I_1 and I_2 in terms of I_x and I_{BD}:

$$I_{out} = I_1 + I_2 = \sqrt{4I_x^2 + I_{BD}^2} \simeq |I_{BD}| \text{ if } I_{BD} \gg I_x$$

The previous analysis assumes no body effect in the transistors involved in the translinear loop. This would need the implementation of transistors in a separate well. However, extensive circuit simulations using accurate subthreshold MOS models [12] have revealed that by using the body effect of transistor M9, the condition $I_{BD} \gg I_x$ can be more relaxed. The simulated performance of the circuit described in Fig. 4, where transistor M9 has no independent well, is illustrated in Fig. 5. As clearly shown, even if the I_x current is comparable

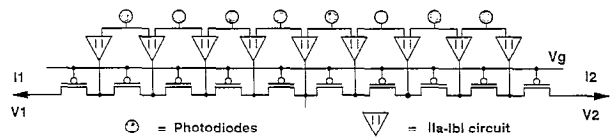

Fig. 6. Architecture for contrast-sensitive PSDs.

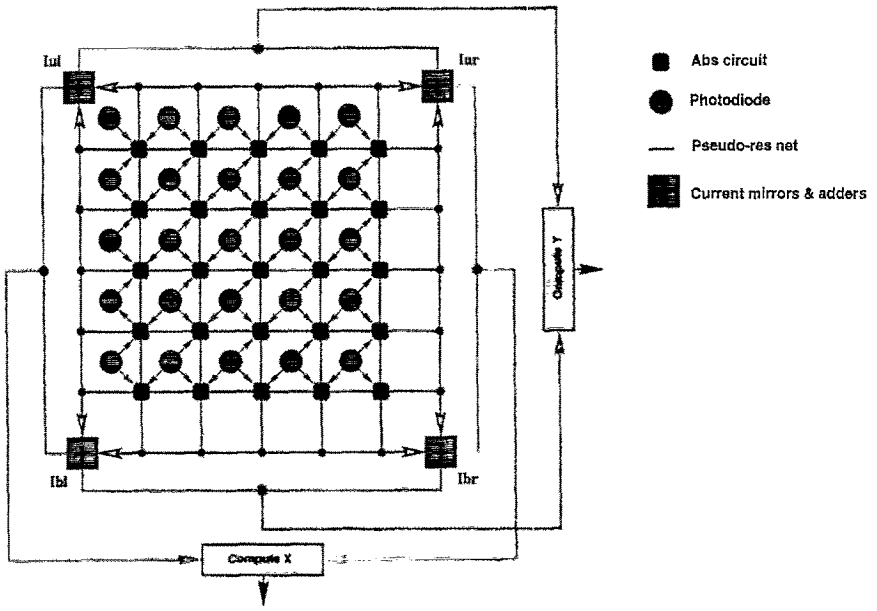

Fig. 7. 2-D implementation.

to I_{BD}, the circuit displays low offset current and good linearity.

In order to get an edge-based PSD, a network like the one shown in Fig. 6 can be used to make the absolute value of the gradient in one dimension. A 2-D architecture can easily be arranged as shown in Fig. 7 to get a similar result. An array of absolute-value circuits is placed in the internodal points of a photodiode matrix. Each absolute value circuit takes the photocurrents from the two upper-left photodiodes and the output current is sinked into a pseudo-resistive 2-D grid. If I_{UR}, I_{UL}, I_{BR}, I_{BL} are the output currents at the upper-right, upper-left, bottom-right, and bottom-left of the array, respectively, the first-order moment of the distribution is given by [6]

$$\frac{x}{L}=\frac{I_{UR}+I_{BR}-I_{BL}-I_{UL}}{I_{UR}+I_{BR}+I_{BL}+I_{UL}} \tag{3a}$$

$$\frac{y}{L}=\frac{I_{UR}+I_{UL}-I_{BL}-I_{BR}}{I_{UR}+I_{BR}+I_{BL}+I_{UL}} \tag{3b}$$

where L is again the device length and height. Referring to Fig. 7, four current mirrors are duplicating the corner currents, so that each one can be used for the x and y centroid coordinates. For the final computation, two circuits like the one described in Fig. 2 are used for the vertical and horizontal coordinates.

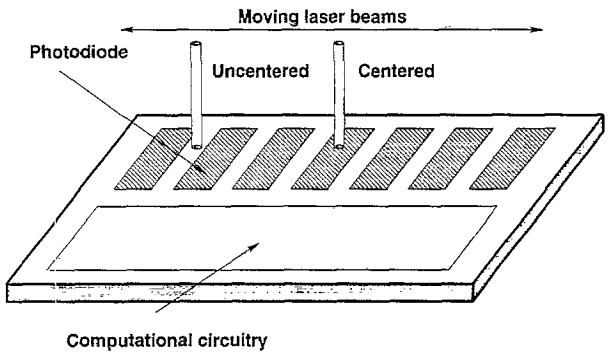

Fig. 8. Testing the sensor.

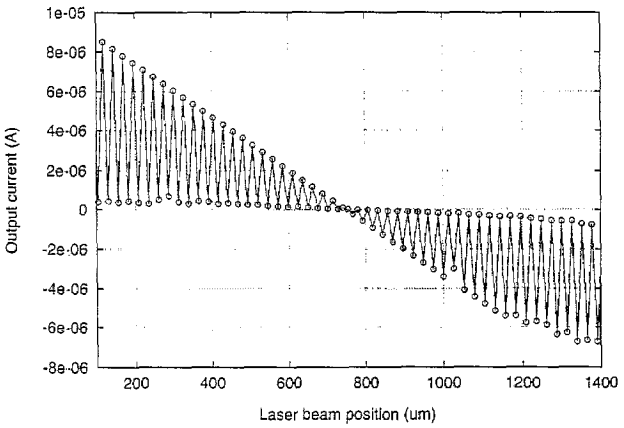

Fig. 9. Experimental data at low optical power (250 nW).

3. Experiments and results

A chip prototype containing the circuits of Fig. 1(b) and Fig. 2 along with a photodiode array has been fabricated in the 2 μm BiCMOS MOSIS process. The photodiode strip is composed of 53 cells and it is 1300 μm long. The active area of each photodiode is 45 μm × 10 μm. To verify the linearity of the output with respect to the position of a light spot, a He–Ne laser of 632.8 nm wavelength has been used. A computer-controlled system has been used to move the laser beam mechanically along the array as displayed in Fig. 8. The moving step was set to alternately center the photo-site and the internodal point as displayed in the same Figure. A first set of output data, by using 250 nW of optical power, is plotted

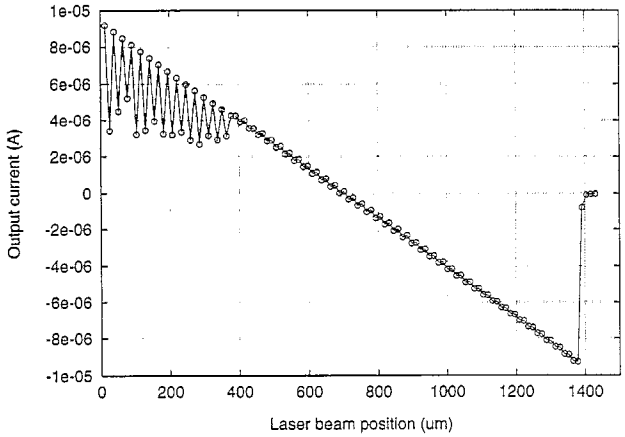

Fig. 10. Experimental data at higher optical power (1.5 μW): raw data.

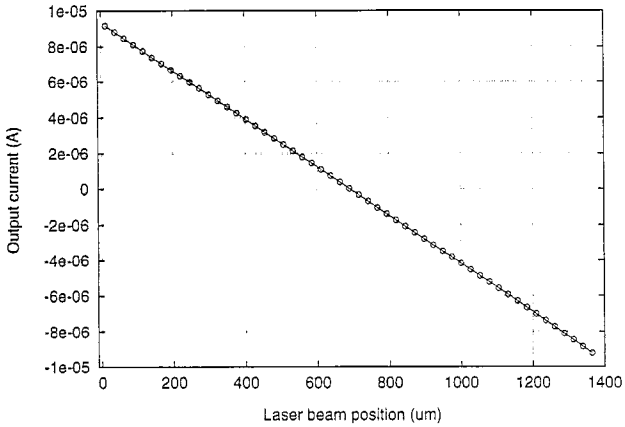

Fig. 11. Experimental data at higher optical power (1.5 μW): centered data set.

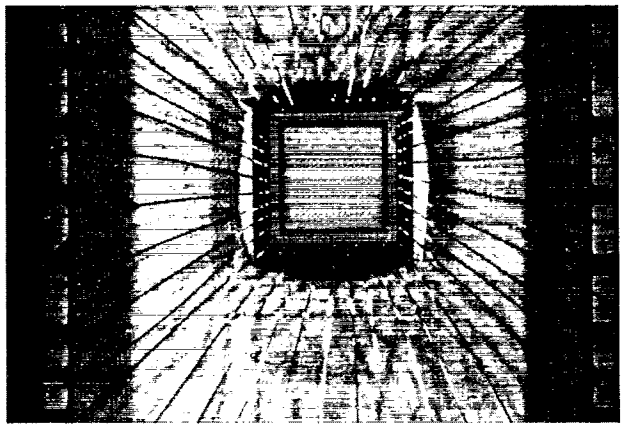

Fig. 12. Die photograph.

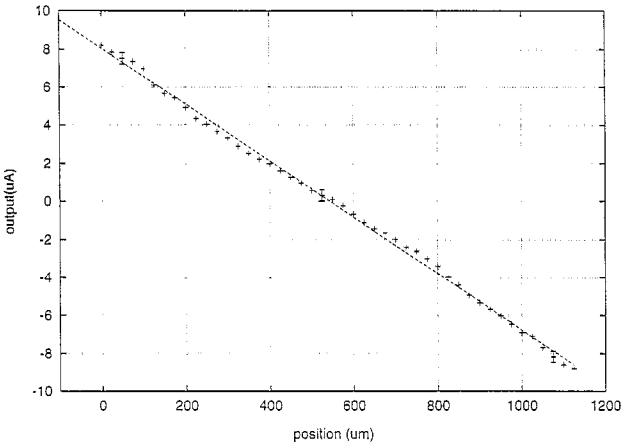

Fig. 13. Experimental data for the edge-sensitive PSD.

in Fig. 9, where the bias current of the computational block has been set to 10 μA. Notice how the uncentered set gives quasi-zero output while the centered one lies on a line. The deviation from the expected behavior of the far-right data is due to the small amount of collected photocurrent that causes a drop of the current gain in bipolar transistors. This behavior is particularly apparent for optical powers below 400 nW. To overcome this problem a MOS source follower stage can be placed to buffer the B1–B2 pair with respect to the diode-connected transistors, even though this approach may slow down the speed of the sensor. When a higher optical power (1.5 μW) is used, as displayed in Fig. 10, the sensor performance increases. Due to the blurring effect of the passivation oxide and to the difficulty of keeping a stable laser beam size during the movement, the spot diameter regarding the right-side data is larger than the pitch. In this case, the circuit automatically computes the center-of-mass position showing no distinction between centered and uncentered data, as displayed in the left-side of the plot. By taking into account even data only, the plot of Fig. 11 is obtained. Measurements of this kind performed on the whole chip set displayed a non-linearity r.m.s. error over the full range of below 0.1%.

To verify the performance of the circuits described in Fig. 4, a 1-D and a 2-D edge-sensitive PSDs as described in the previous section have been implemented and tested. The 1-D array is 1350 μm long and the pitch is 30 μm. The 2-D pixel pitch is 90 μm, is composed of 14×12 elements and its microphotograph is shown in Fig. 12. To measure the performance, a dark edge has been moved along the 1-D and 2-D arrays in order to check the sensor capability of tracking edges. A typical result is displayed in Fig. 13 for the 1-D PSD, where the bias current of the computational block has been set to 10 μA. Similar plots can be drawn for the 2-D chip at a smaller resolution. As clearly shown, the sensor is able to track the moving edge instead of the centroid of the bright shape. Measurements over the chip set have revealed a non-linearity r.m.s. error below 1.2% with respect to the full range.

Unfortunately, a careless design of the layout has led to a misbehavior of both 1-D and 2-D edge-sensitive sensors due to a permanent current injection at one extremum when illuminated. More specifically, if the latter experiment was performed with exchanged dark and bright edges, it would give qualitatively different results from the ones plotted in Fig. 13, since the above-mentioned extremum is illuminated by the bright side of the edge.

4. Conclusions

A new compact position-sensitive circuit has been presented and experimentally evaluated. The feasibility of using standard MOS devices for detecting light and for computing position has been demonstrated. Results in terms of linearity have shown very good performance, comparable to those for sensors implemented in more sophisticated technology. A new scheme to implement edge-sensitive PSDs has been investigated and two (1-D and 2-D) implementations have been designed and tested. Despite layout errors that prevent a full test of the edge-sensitive structure, the capability of tracking oriented edges has been demonstrated.

Acknowledgements

We are very grateful to D. Marx and to Professor D. Psaltis for their help in providing the optical test equipment. This work is supported in part by the Center for Neuromorphic Systems Engineering as a part of the National Science Foundation Engineering Research Center Program, and by the California Trade and Commerce Agency, Office of Strategic Technology.

References

[1] A.K. Dutta, Y. Hatanaka, Design and performance of the mesh-type high-speed silicon optical position-sensitive devices, IEEE Trans. Electron. Devices 38 (1991) 498–504.
[2] H. Muro, P.J. French, An integrated position sensor using JFETs as a buffer for PSD output signal, Sensor and Actuators A21–A23 (1990) 544–552.
[3] T. Smith, J.H. Huijsing, An integrated linear position sensitive detector with digital output, Tech Digest, 6th Int. Conf. Solid-State Sensors and Actuators (Transducers '91), San Francisco, CA, USA, 24–28 June, 1991, pp. 719–721.
[4] C. Mead, Analog VLSI and Neural Systems, Addison-Wesley, Reading, MA, 1989.
[5] A. Andreou, K. Boahen, P. Pouliquen, A. Pavasovic, R. Jenkins, K. Strohbehn, Current-mode subthreshold MOS circuits for analog VLSI neural systems, IEEE Trans. Neural Networks 2 (1991) 205–213.
[6] D.L. Standley, An object position and orientation IC with embedded imager, IEEE J. Solid State Circuits 26 (1991) 1853–1858.
[7] P. Venier, O. Landolt, P. Debergh, X. Arreguit, Analog CMOS Photosensitive Array for Solar Illumination Monitoring, Tech. Digest, IEEE Int. Solid-State Circuits Conf., San Francisco, CA, USA, Feb. 1996, pp. 96–97.
[8] M. Tartagni, P. Perona, Computing centroids in current-mode technique, Electron. Lett. 29 (1993) 1811–1813.
[9] X. Vitoz, X. Arreguit, Linear networks based on transistors, Electron. Lett. 29 (1993) 297–299.
[10] C. Toumazou, F. Lidgey, D. Haigh, Analogue IC Design: The Current Mode Approach, IEE, Peter Peregrinus, London, 1990.
[11] M. Ismail, T. Fiez, Analog VLSI – Signal and Information Processing, McGraw-Hill, New York, 1994.
[12] D. Gillespie, J. Lazzaro, An Introduction to LOG with AnaLOG, Caltech VLSI CAD Tool Distribution, 1993, v.5.10.

Biographies

Marco Tartagni received the five-year degree in electrical engineering (Laurea in Ingegneria Elettronica) in 1988 from the University of Bologna, Italy, and the Ph.D degree in electrical engineering and computer sciences in 1993 from the same university. He joined the Department of Electrical Engineering of the California Institute of Technology, Pasadena, CA, in 1992 as a visiting student and in 1994 as a research fellow, working on various aspects of analog VLSI for image processing. Since March 1995 he has been a research associate at the Department of Electronics of the University of Bologna. His current research interests include integrated sensors, low-power electronics, and current-mode circuit design.

Pietro Perona received a doctor in engineering degree from the University of Padua in 1985 and a Ph.D. in electrical engineering and computer science from the University of California at Berkeley in 1900. He is currently professor of electrical engineering at the California Institute of Technology and adjunct professor at the University of Padua. His main research interests are computational vision and psychophysics and modelling of human vision.